REMARKS

In the first office action, the examiner has entered the following objections:

- Figures 1 and 2 of the drawings were objected to because of minor informalities. These have now been corrected on the Replacaement Sheets, and the changes are shown on the Annotated Sheets.
- Claims 3, 14, 15 and 22 were objected to on the basis of certain repetitive statements and phrasings. These, along with the specification, have all been corrected by amendment.

The examiner then issued a rejection of claims 1-8 and 10-21 under 35 USC §103(a) as being obvious and thus unpatentable over Lakshmanamurthy et al (US2004/0004964) (hereinafter Lakshmanamurthy) in view of Elmaliach et al (US patent 6,922,732) (hereinafter Elmaliach). Claims 9, 23 and 24 are rejected under 35 USC §102(e) as anticipated by Lakshmanamurthy.

As a general overview, some of the distinctions between the Lakshmanamurthy application and the present claimed invention are noted as follows. In the first place, this reference relates to a network processor design in which data segments are received from a switch fabric for assembling into full packets. In this network processor environment, the processing elements examine the data segments by putting the segments into appropriate buffers in memory.

In the present invention, a pipeline configuration is described for use in network traffic management for the hardware scheduling of events arranged in a hierarchical linkage. The pipeline configuration does not examine packet data nor does it provide a packet assembling function.

The DRAM and SRAM devices described in Lakshmanamurthy are used for centralized storage to store data segments of full packets as well as context for assembling data segments belonging to given full packets.

However, the DRAM and SRAM storage devices described in applicants' invention are arranged so as to minimize the use of more costly SRAM, and are specific for network traffic scheduling function only.

The pipeline described in Lakshmanamurthy comprises different processing stages that relate to the packet reassembling functions. Switching of pipeline stages occurs when all data segments belonging to a full packet are received and stored in the memory location.

On the other hand, the pipelines described in the present application are to arrange access windows for SRAM and DRAM accesses for each scheduled events such that there are no conflicts in accessing the memory resources among different scheduling events.

The virtual output queues/connections described in Lakshmanamurthy are used to identify the context for the reassembling packets but not for network traffic scheduling purposes.

Conversely, the flow queues described by applicants are used to enforce network traffic management such that the utilization of network resources can be fully optimized.

In summary, this prior art reference (Lakshmanamurthy) is not relevant to the present invention in terms of functions and applications.

Turning next to the secondary Elmaliach patent, it should be noted that this patent describes a class-based per flow queuing for use with multiple link-sharing hierarchies. It includes a new queuing decision layer that considers all hierarchies simultaneously by pre-distributing tokens into each hierarchy such that the traffic injected by each flow queue into the network are limited to the tokens allocated for the flow queues. This prior art is a network flow control mechanism which prevents the flow queues from overloading the shared network resources. This method of managing bandwidth on hierarchical links is a credit-based method. As such, it first assigns a set of tokens to each resource, and then performs simple resource scheduling based on the accumulated tokens.

As differentiated from Elmaliach, the captioned invention uses a calendar to perform per flow network traffic scheduling functions. The invention is related to the arrangement of pipelining accesses to SRAM and DRAM devices to minimize hardware system implementation costs. The novel method of managing bandwidth on hierarchical

links is a calendar-based method. It is driven by a single scheduling stage that reads a predefined calendar to service resources.

In summary, the patent to Elmaliach is related to an algorithm of limiting flow queues from overloading the shared network resources whereas the present invention relates to hardware implementation for cost reduction by implementing the memory devices access pipeline.

The various prior art rejections will now be discussed in more detail as follows.

FIRST PRIOR ART REJECTION

Claims 1-8 and 10-21 are rejected under 35 USC 103(a) as being unpatentable over Lakshmanamurthy in view of Elmaliach.

The rejection of claim 1 depends on the combined teachings of the two references, the first of which relates to the assembly of full packets from data segments. This first reference is totally silent as to the use of the pipeline arrangement for a network traffic scheduler and, as acknowledged by the examiner, it is also silent about a hierarchical arrangement. Although the secondary reference does discuss link sharing hierarchies, it manages bandwidth using a credit-based method. This is totally different from the present invention in which control blocks are accessed on an approximate fixed period of time.

Thus, claim 1 has been amended to reflect the fact that the present invention does not utilize tokens such as used in a credit based system, which is the focus of the Elmaliach patent. Instead, the claim now specifies the use of time based calendar arrays and weighted fair queuing calendar arrays for allocating bandwidth. Furthermore, the claim has been modified by incorporation of the subject matter of claim 6 that specifies that the memory access allocated to enqueue tasks does not conflict with memory access allocated to dequeue tasks. This further distinguishes the present invention as now claimed in independent claim 1 from the cited and applied references. Accordingly, withdrawal of the obviousness rejection is respectfully requested.

The Federal Circuit Court has consistently held that when obviousness is based on the teachings of multiple prior art references, some "suggestion, teaching, or motivation" should be established that would lead a person of ordinary skill in the art to combine the

relevant prior art teachings in the manner claimed. See for example Tec Air, Inc. v Denso Mfg. Mich. Inc., 192 F.3d 1353, 1359-60. (Fed. Cir. 1999). This criterion has been used by the Federal Circuit for the past quarter of a century, and has been consistently applied or acknowledged by numerous panels containing several currently active members of the court.

The "suggestion to combine" requirement stands as a critical safeguard against hindsight analysis and rote application of the legal test for obviousness. See Yamanouchi Pharmaceutical Co., Ltd, v. Danbury Pharacal, Inc., 231 F. 3d 1339, 1343 (Fed. Cir. 2000). By employing this safeguard, the claims in question cannot be used as a guide through plural prior art references, combining the right references in the right way so as to deny their patentability or enforceability.

Recently engrafted onto this test used by the CAFC is the Supreme Court pronouncement in KSR International Co. v. Teleflex, Inc. (Decided April 30, 2007) that the obviousness analysis should likewise consider whether one skilled in the art could implement a predictable variation to the prior art. If so, this predictability could defeat patentability under 35 USC §103. Applicants respectfully submit that the invention as now claimed does not represent a "predictable variation" of the known prior art. Thus, one skilled in the art, without knowledge of the contents of this pending application, would not likely implement such a variation without the use of sufficient inventiveness to warrant patent protection under 35 USC §103(a). Accordingly, the rejection based on obviousness should be withdrawn.

Inasmuch as claims 2-5 and 7-8 all depend from claim 1 and further limit the scope of the invention as spelled out in this independent claim as amended, these dependent claims all should be considered to be allowable as well.

Skipping over to claim 12, applicants respectfully submit that this independent claim has now been amended so as to clearly distinguish over the combined prior art. In the first place, the examiner indicates that "at least some of the memory devices" of Lakshmanamurthy store "more than one type of control block". Yet applicants respectfully submit that the quoted portions of the specification and Figures 1 and 4 of this reference do not support such a teaching. Furthermore, the amendments to this claim 12 provide unquestioned support for patentability. The claim now specifies that the pipeline arrangement serves the multiple queues within an approximated fixed period of

time using both time based calendar arrays and weighted fair queueing calendar arrays for allocation of available bandwidth.

Claims 13-18 all depend from claim 12 which has now been substantially amended to place it in condition for allowance. Accordingly, these dependent claims should be deemed to be allowable as well.

SECOND PRIOR ART REJECTION

Claims 9 and 22-24 are rejected under 35 USC 102(e) as being anticipated by Lakshmanamurthy.

Turning first to claim 9, applicants have now amended this claim so as to render it clearly distingishable over the applied reference. The claim has been amended to reflect that the informaion to be retrieved is present in either a hierarchical link sharing mode or a non-hierarchical link sharing mode. This feature is not taught by the anticipation reference. Furthermore, the method now includes a step of avoiding conflicts between enqueue and dequeue memory accesses and the additional steps of using both time based and weighted fair queueing calendar arrays for bandwidth allocation. These claim limitations serve to further distinguish over the patent publication reference. Accordingly, claim 9 clearly contains allowable subject matter and should be allowed.

Applicants respectfully submit that the rejection of claims 22-24 has been favorably resolved by substantial amendments to independent claim 22 and cancellation of claims 23 and 24. Claim 22 now succinctly specifies that the computer readable program has the ability to control the storage location of block content in either SRAM or DRAM, and to select a flow queue to egress based on a time-based or a weighted fair queueing calendar. These features are not disclosed nor suggested by Lakshmanamurthy. Accordingly, the subject matter of claim 22 clearly is distinguishable over the reference, and this claim should be allowed.

It is well recognized that prior art is anticipatory only if every element of the claimed invention is disclosed in a single item of prior art in the form literally defined in the claim. Jamesbury Corp. v. Litton Indus. Products, 756 F.2d 1556, 225 USPQ 253 (Fed. Cir. 1985); Atlas Powder Co. v. du Pont, 750 F.2d 1569, 224 USPQ 409 (Fed. Cir. 1984); American Hospital Supply v. Travenol Labs, 745 F.2d 1, 223 USPQ 577 (Fed.

Cir. 1984). Inasmuch as the applied reference does not disclose every item now defined in the claim, anticipation does not exist.

CONCLUSION

Applicants respectfully submit that the amendments to the claims now place the application in condition for allowance. Furthermore, the amendments to the drawings overcome the examiner's objections. The examiner is respectfully requested to enter this Amendment and to take such additional action as may be consistent therewith.

If there are any minor matters that can easily be resolved by phone or by email, the Examiner is encouraged to contact the undersigned as a step toward resolution. Consideration and entry of this amendment is respectfully requested.

Respectfully submitted,

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